ABSTRACT

The invention describes structures and a process for providing ESD protection between multiple power supply lines or buses on an integrated circuit chip. Special diode strings are used for the protection devices whereby the diodes are constructed across the boundary of an N-well and P substrate or P-well. The unique design provides very low leakage characteristics during normal circuit operation, as well as improved trigger voltage control achieved by stacking 2 or more diodes in a series string between the power buses.